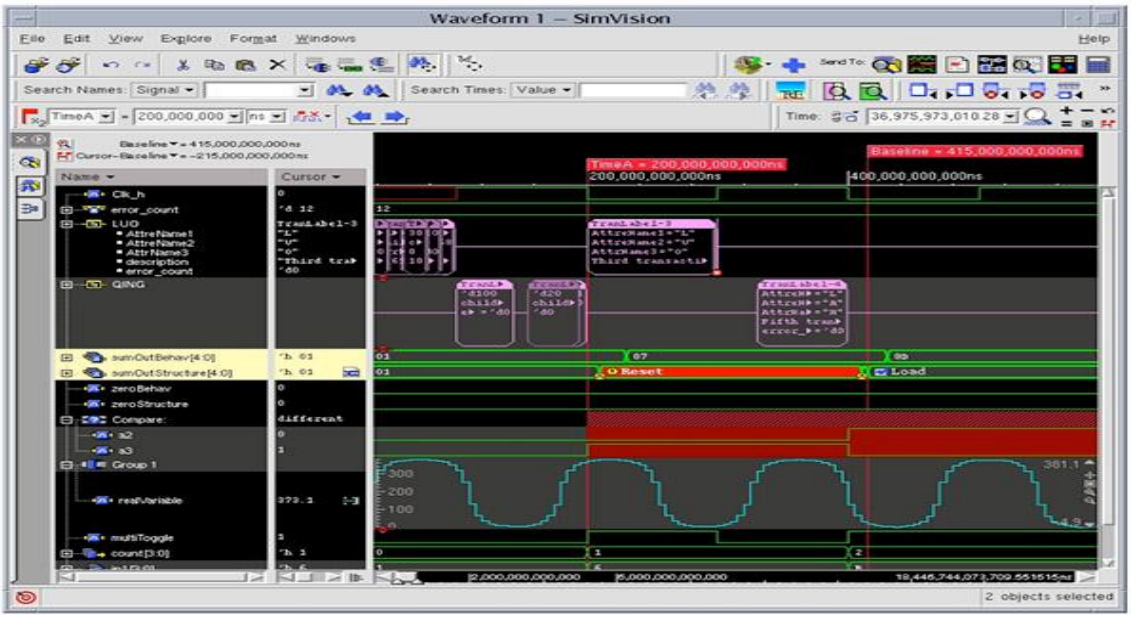
Karunya INSTITUTE OF TECHNOLOGY AND SCIENCES
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1956)
MoE, UGC & AICTE Approved; NAAC Accredited A++
Karunya Nagar, Coimbatore - 641 114, Tamil Nadu, India.

DIVISION OF ELECTRONICS AND COMMUNICATION ENGINEERING

VLSI LABORATORY

1. CADENCE UNIVERSITY STANDARD BUNDLE



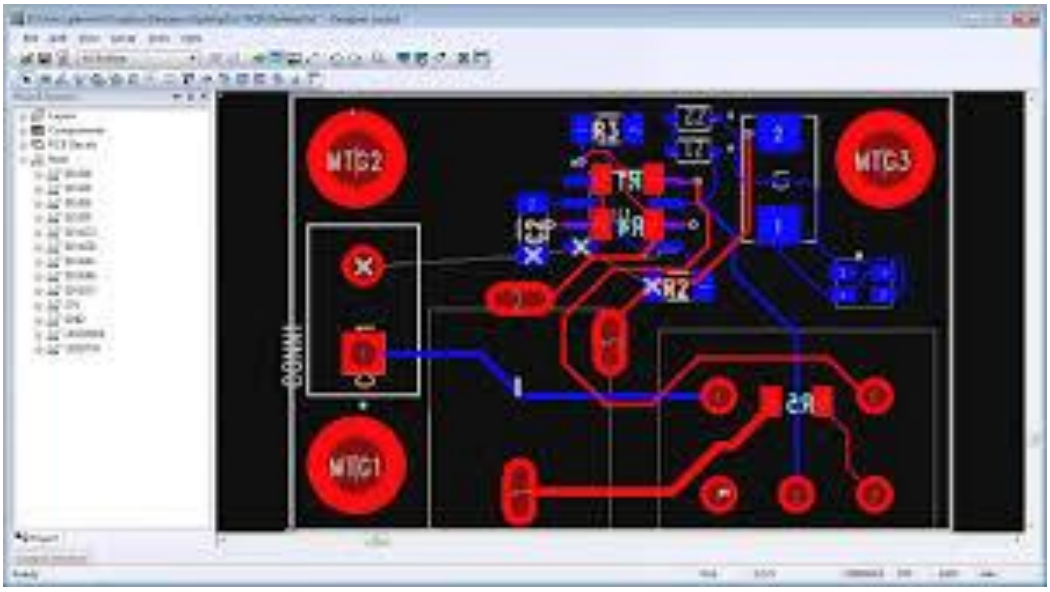
License Type	3 Years
No. of Users	20
Tool Bundle	• Conformal® Low Power GXL • GenusTM Low Power Option • GenusTM Synthesis Solution • Cadence® SKILL Development Environment • Virtuoso® AMS Designer Environment • Virtuoso® Schematic Editor XL • Virtuoso® ADE Assembler • Virtuoso® Layout Suite GXL • VoltusTMTM-Fi Custom Power Integrity Solution XL • InnovusTM Implementation System • JasperGold® Formal Verification Platform • Modus DFT ATPG • InnovusTM DFM Option • Generator to generate Assura® compatible verification decks • Pcell Generator • Cadence® QuickView Layout and Mask Data Viewer • Cadence® Physical Verification System Design Rule Checker XL • Cadence® PVS Layout vs Schematic Checker XL • Cadence® Physical Verification System QuickView Signoff Environment

	• Virtuoso® Integrated PVS Option for Layout Suite • Advanced SI & PI • Allegro® PCB Designer • Spectre® AMS Designer • Spectre® Multi-Mode Simulation with AMS • VoltusTM IC Power Integrity Solution XL (VTS-XL) • TempusTM Timing Signoff Solution ECO • vManagerTM Project Server • vManagerTM Linux Client • XceliumTM Single Core

Applications

- ✓ Mixed - mode Simulation & Synthesis
- ✓ Analog Simulation (Schematic to GDS II)
- ✓ Digital Simulation (RTL to GDS II)
- ✓ Technology – 45nm, 90nm, 180nm

2. MENTOR GRAPHICS HEP - I & II

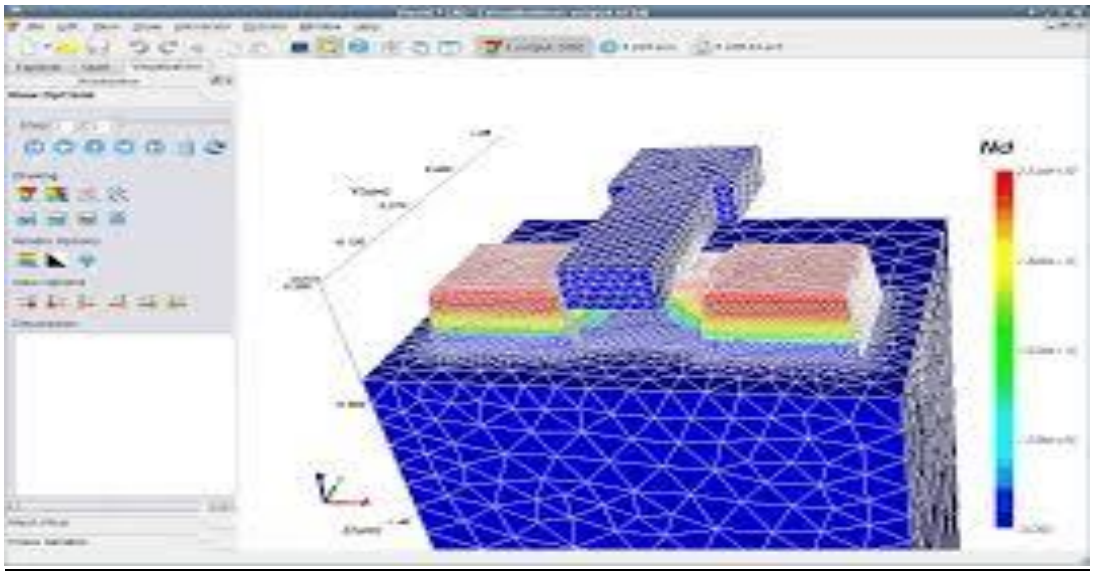


License Type	3 Years
No. of Users	33
Tool Bundle	**Mentor Graphics HEPCategory1** • ADiTTM , Eldo® • QuestaTM ADMS • PyxisTM , Calibre® • IE3D **Mentor Graphics HEP Category 2** • VistaTM, • ReqTracerTM, • Questa (including ModelSim®) • Precision Synthesis • Leonardo SpectrumTM ASIC • TessentTM Silicon Test • Questa Codelink • SystemVisionTM • Bridgepoint®

Applications

- ✓ Design Architech for Schematic design
- ✓ IC Station for Layout design
- ✓ Accusim for Analog Simulation
- ✓ Post –Layout Simulation and Verification till GDS-II file generation
- ✓ Technology – 130nm

3. AsiaPac Advanced TCAD University Bundle

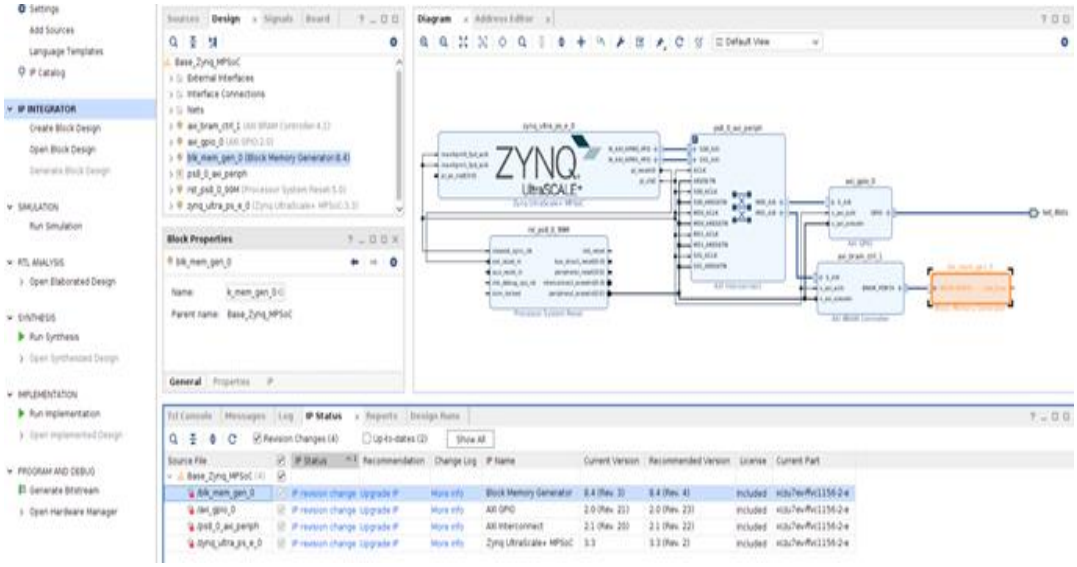


License Type	3 Years
No. of Users	4
Tool Bundle	IC WorkBench Edit/View Plus TCAD Sentaurus Workbench / Workbench Advanced TCAD Sentaurus Process/ Process 3D TCAD Sentaurus Device / Device Advanced TCAD Sentaurus Device DSM / Compound /3D TCAD Sentaurus Parallel TCAD Sentaurus Device EMW/ Monte Carlo /Power TCAD Sentaurus PCM Studio/ PCM Library TCAD Sentaurus Structure Editor /3D TCAD Sentaurus Process Kinetic MC TCAD-Taurus-Medici /TSuprem4 /Raphael TCAD Sentaurus Visual Sentaurus Process Explorer

Applications

- ✓ Device Modeling and Simulation
- ✓ Analysing DC Characteristics of a Device
- ✓ Performing RF Simulation of Device
- ✓ Conducting breakdown Simulations
- ✓ Performing Optical Simulations

4. XILINX Vivado Design Suite 19.2



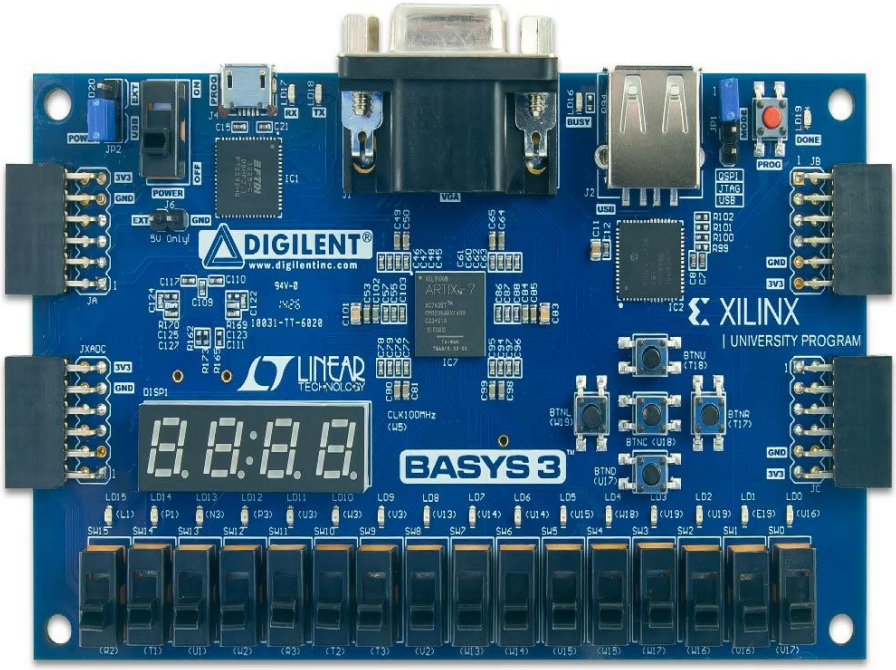
License Type	Perpetual
No. of Users	50
Tool Bundle	• IDE Enhancements • Model Composer • IP Integrator • IP Enhancements • SmartConnect Enhancements • URAM Readback/Writeback IP for UltraScale+ Devices • HBICAP • Video and Imaging IPs • RTL Synthesis • Implementation • Dynamic Function eXchange (DFX) • Implementation Design Flow • Design Analysis and Timing Closure • Incremental Compile • Vivado Simulator

Applications

The Vivado design suite is the set of tools provided by Xilinx and is used to design, program, and debug Xilinx's line of FPGAs

- ✓ Digital System Design flow
- ✓ RTL Simulation & Synthesis
- ✓ Real-time FPGA Implementation
- ✓ Programming and Debugging

5. FPGA – Basys 3



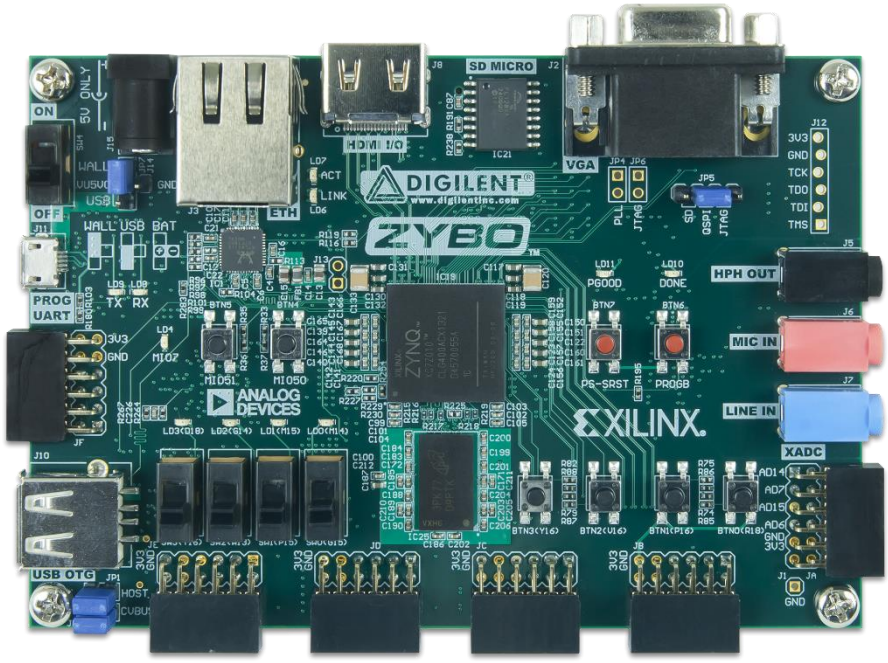
Make	Digilent
Part Number	XC7A35T-1CPG236C
Device Family	Artix -7
Features	• Designed Exclusively for Vivado Design Suite. Expanded features are available through purchase of the Design Edition. • Digilent USB-JTAG port for FPGA programming and communication • On-chip analog-to-digital converter (XADC) • Internal clock speeds exceeding 450 MHz • 90 DSP slices • Five clock management tiles, each with a phase-locked loop (PLL) • 1,800 Kbits of fast block RAM • 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops) • 4 Pmod ports: 3 Standard 12-pin Pmod ports, 1 dual purpose XADC signal / standard Pmod port • 4-digit 7-segment display • 5 user pushbuttons • 16 user LEDs

	• 16 user switches • USB HID Host for mice, keyboards and memory sticks • 12-bit VGA output • USB-UART Bridge • Serial Flash

Applications

- ✓ Digital System Design
- ✓ Implementation of System in Real time
- ✓ Parameters measurement.

6. FPGA – Zybo Zynq 7000



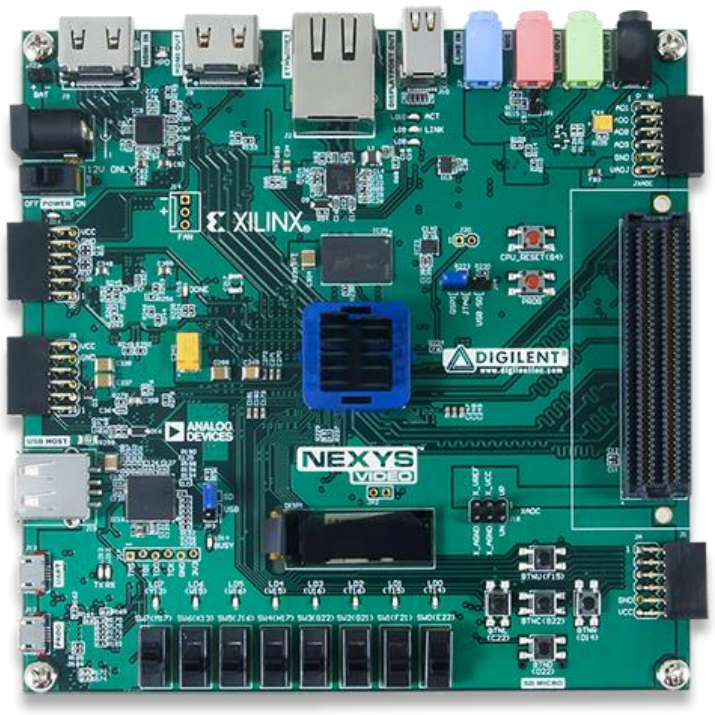
Make	Digilent
Part Number	XC7Z010-1CLG400C
Device Family	Dual-core ARM Cortex-A9 processor with Xilinx 7-series
Features	• 667MHz dual-core Cortex-A9 processor • DDR3L memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports • High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO • Low-bandwidth peripheral controller: SPI, UART, CAN, I2C • Programmable from JTAG, Quad-SPI flash, and microSD card (Micro B USB cable **NOT** included). • Programmable logic equivalent to Artix-7 FPGA • 1 GB DDR3L with 32-bit bus @ 1066 MHz • 16 MB Quad-SPI Flash with factory programmed 128-bit random number and 48-bit globally unique EUI-48/64™ compatible identifier • Gigabit Ethernet PHY • HDMI sink port (input) with CEC (Zybo Z7-20) and without CEC (Zybo Z7-10) • HDMI source port (output) with CEC • Audio codec with stereo headphone, stereo line-in, and microphone jacks • 6 push-buttons • 4 slide switches

	• 5 LEDs • 2 RGB LEDs • 6 Pmod ports on the Zybo Z7-20

Applications

- ✓ Digital System Design
- ✓ Implementation of System in Real time
- ✓ Parameters measurement.

7. FPGA – Nexys Video



Make	Digilent
Part No	XC7A200T-1SBG484C
Device Family	Artix -7
Features	• 33,650 logic slices, each with four 6-input LUTs and 8 flip-flops • Close to 13 Mbits of fast block RAM (3x more than the Nexys 4 DDR) • Ten clock management tiles, each with phase-locked loop (PLL) • 740 DSP slices • Internal clock speeds exceeding 450 MHz • On-chip analog-to-digital converter (XADC) • Up to 3.75Gbps GTP transceivers • 8 user switches • USB-UART Bridge • HDMI Sink and HDMI Source • 6 user push buttons • 512MiB 800Mt/s DDR3 • Pmod for XADC signals • 8 user LEDs • 160-pin FMC LPC connector • DisplayPort Source • User EEPROM • Serial Flash

	• Digilent Adept USB port for programming and data • 128×32 monochrome OLED display • MicroSD card connector • Audio codec w/ four 3.5mm jacks • 10/100/1000 Ethernet PHY • Four Pmod ports • USB HID Host for mice, keyboards and USB MSD Host

Applications

- ✓ Digital System Design
- ✓ Implementation of System in Real time
- ✓ Image Processing
- ✓ Parameters measurement.

VLSI LABORATORY				
				Total Investment: ₹. 19150705.00
Sl.No	**Name of the Equipment**	**Quantity**	**Amount (Rs.)**	**Date of Purchase**
	HARDWARE			
1	Lattice Isp	1	105820.00	05.09.00
2	Embedded Development Kit	3	71280.00	12.05.03
3	Universal Vlsi Development System	5	110500.00	12.05.03
4	Spartan 2e	6	122100.00	12.03.03
5	Virtex2p With Accessories	5	204570.00	29.03.08
6	Virtex 4	1	55550.00	29.03.08
7	Virtex5(Opsparc)	1	59424.00	30.11.10
8	Virtex5(Genesys)	1	48620.00	30.11.10
9	Basys 3	18	163601.00	20.02.18
10	ZYBO	3	55224.00	20.02.18
11	Nesys 4 Video	1	36816.00	20.02.18
12	Interface Kit	33	63016.00	20.03.03
13	University Trainer Kit	4	37400.00	29.03.08
14	Mic	2	8600.00	22.10.10
15	Computer – Hp	20	540000.00	19.11.08
16	Computer – Hp	18	667368.00	30.09.09
17	Computer - Lenovo	8	336000.00	11.06.12
18	Computer - Lenovo	10	285000.00	07.12.13
19	Laser Printer	1	10723.00	12.08.04
20	Camera	1	6750.00	10.02.09
21	Camera - logitech	1	2720.00	12.08.04
22	Image Processing Kit	1	217434.00	13.11.01
23	AD/DA Card	1	7200.00	10.10.01
24	Tms320c50 Trainer	4	44400.00	22.08.02
25	Tms320c33 Trainer	2	47654.00	05.05.04

26	Tms320c50 Starter Kit	3	39000.00	22.08.02
27	Tms320c5416 Starter Kit	6	147000.00	31.03.03
28	Adsp 2181	1	35643.00	31.03.03
29	Tms320vc5410/16 Trainer	10	150000.00	01.03.04
30	Vsmps	3	25008.00	03.05.04
31	Printer	1	10723.00	12.08.04
32	Lcd Screen With Kit	1	29200.00	21.11.08
33	Ethernet Switch	4	9600.00	10.04.03
34	Ethernet Switch	1	1520.00	10.04.03
35	Monitor (Led-Lv1911)	1	6500.00	02.08.14
36	Blower	1	4610.00	17.03.04
37	Laser Printer (M1005)	1	16200.00	06.02.19
38	Computer -Dell	1	75255.00	01.04.19
39	Computer -Dell	5	413221.00	31.05.21
	SOFTWARE			
	Name Of The Software	**User**	**Cost(Rs.)**	**Date of**
40	Tanner Tools Pro	5	266448.00	19.01.05
41	Mentor Graphics EDA Tools	5	208400.00	09.05.05
42	Mentor Graphics HEP (I&II) Renew &	33	990000.00	04.10.06
43	Mentor Graphics HEP (I&II) Renew &	33	312000.00	17.02.09
44	Mentor Graphics HEP (I&II) Renew &	33	315000.00	10.11.11
45	Mentor Graphics HEP (I&II) Renew &	33	495850.00	21.11.13
46	Mentor Graphics HEP (I&II) Renew &	33	531000.00	10.01.18
47	Mentor Graphics HEP (I&II) Renew &	33	619500.00	28.12.20
48	VIVADO Design suite	50	147700.00	21.11.13
49	VIVADO Design suite - Renew & Upgr	50	218300.00	04.03.20
50	Synopsys Asia Pacific	5	550000.00	31.03.09
51	Synopsys Asia Pacific - Renew & Upgr	4	559851.00	28.11.12
52	Tcad Asia Pacific	1	275000.00	31.03.09
53	Tcad Asia Pacific- Renew & Upgr	3	710856.00	30.04.12
54	Tcad Asia Pacific- Renew & Upgr	3	945000.00	12.05.15
55	Tcad Asia Pacific- Renew & Upgr	3	1180000.00	03.10.18

56	Tcad Asia Pacific- Renew & Upgr	4	1180000.00	29.10.21
57	Cadence University Bundle	10	1102500.00	28.11.11
58	Cadence – Renew & Upgr	10	1287100.00	09.12.14
59	Cadence – Renew & Upgr	10	1431340.00	20.12.17
60	Cadence – Standard bundle	20	885000.00	15.12.20
61	Cadence – Standard bundle	30	1026000.00	19.12.23

Research Publications

Scopus / Web of Science Indexed Journals

S.No	Name of the Faculty & Designation	Title of article	Name of the Journal	Volume No., Page No., Year / Month of Publication	Citation Index / Impact Factor
1	Princy Prince, N.M.Sivamangai	A novel technique for minimisation of March test using read equivalent stress	International Journal of Nanomanufacturing	https://doi.org/10.1504/IJNM.2020.106334	0.33
2	D.S.Shylu Sam, P.Sam Paul, D. D. Jackuline Moni, Arolin Monica	A power efficient delta-sigma ADC with series-bilinear switch capacitor voltage-controlled oscillator	Telkomnika (Telecommunication Computing Electronics and Control)	DOI: 10.12928/TELKOMNIKA.v18i5.14034, 18(5), pp. 2618-2627,2020	----
3	Dr. D. Nirmal	Analytical Model of Double Gate Stacked Oxide Junctionless Transistor Considering Source/Drain Depletion Effects for CMOS Low Power Applications	Silicon	https://doi.org/10.1007/s12633-019-00280-9	1.246
4	Dr. D. Nirmal	On the performance of GaN-on-Silicon, Silicon-Carbide,	International Journal of RF and Microwave Computer-Aided	https://doi.org/10.1002/mmce.22196	1.540

		and Diamond substrates	*Engineering*		
5	S. R.Jino Ramson D.Jackuline Moni S. Vishnu Theodoros Anagnostopoulos · A. Alfred Kirubaraj Xiaozhe Fan	An IoT-based bin level monitoring system for solid waste management	Journal of material Cycles and Waste Management	doi.org/10.1007/s10163-020-01137-9	1.92
6	H.Victor Du John D. Jackuline Moni D.Gracia	A detailed review on Si, GaAs, and CIGS/CdTe based solar cells and efficiency comparison	Electrical Reviews	doi:10.15199/48.2020.12.02	--
7	Dr. D. Nirmal	Variable thermal resistance model of GaN-on-SiC with substrate scalability	Journal of Computational Electronics	DOI: 10.1007/s10825-020-01561-y	1.532
8	Dr. D. Nirmal	Numerical investigation of traps and optical response in III-V nitride quantum LED	Optical and Quantum Electronics,	Volume 52, Issue 12, December 2020, Article number 513, DOI: 10.1007/s11082-020-02633-w,	1.842
9	N.M.Siva Mangai	A novel method for minimizing transient current test time by exploiting RES in SRAM	Analog Integrated Circuits and Signal Processing	http://doi.org/10.1007/s10470-020-01747-1	0.9

10	N.M.Siva Mangai	Electroforming Atmospheric Temperature and Annealing Effects on Pt/HfO2/TiO2/ HfO2/Pt Resistive Random Access Memory Cell	Silicon, Springer	https://doi.org/10.1007/s12633-021-01074-8 25th March 2021	1.49
11	Ajayan, J., Nirmal, D., Mathew, R., Arivazhagan, L., Ajitha, D	A critical review of design and fabrication challenges in InP HEMTs for future terahertz frequency applications,	Materials Science in Semiconductor Processing,	https://doi.org/10.1016/j.mssp.2021.105753, 2021, 128, 105753	------
12	Sridevi, R., Pravin, J.C., Babu, A.R., Nirmal, D	Investigation of Quantum Confinement Effects on Molybdenum Disulfide (MoS2) Based Transistor Using Ritz Galerkin Finite Element Technique	Silicon	DOI: https://doi.org/10.1007/s12633-021-01010-w	1.126
13	Arivazhagan, L., Jarndal, A., Nirmal, D	GaN HEMT on Si substrate with diamond heat spreader for high power applications	Journal of Computational Electronics,	DoI: 10.1007/s10825-020-01646-8	1.431
14	Manoj G	Implementation of FPGA accelerator architecture for	Turkish Journal of Computer and Mathematics	2021, 12(6), pp. 127–135	------

		convolution neural network in emotional recognition system	Education		
15	Shylu Sam , Sam Paul , Diana Jeba Jingle	Design techniques in Carry Select Adder using Parallel prefix adder for improved switching energy	Przegląd Elektrotechniczny	doi:10.15199/48.2021.05.27	-----
16	S.R. Jino Ramson, Member, IEEE, S. Vishnu, A. Alfred Kirubaraj, Theodoros Anagnostopoulos and Adnan M. Abu-Mahfouz, Senior Member, IEEE.	A LoRaWAN IoT enabled Trash Bin Level Monitoring System	IEEE Transactions On Industrial Informatics	DOI 10.1109/TII.2021.3078556, IEEE	9.11
17	Ramson S.R.J.a, b, Moni D.J.c, Vishnu S.b, Anagnostopoulos T.d, Kirubaraj A.A.c, Fan X.a	An IoT-based bin level monitoring system for solid waste management	Journal of Material Cycles and Waste Management	10.1007/s10163-020-01137-9	1.9

Conference Proceedings with ISBN / ISSN

S.No	Name of the Faculty & Designation	Title of the paper	Name of the Conference	Date & Venue
1	Victor Du John. H Jackuline Moni. D	Design Simulation and Comparison of GaAs Single Junction solar cell	2019 5th International Conference on Computing Communication Control and Automation (ICCUBEA)	19-21 st September 2019 pimpri chinchwad college of engineering-Pune
2	Dr. D. Nirmal Associate Professor	Luminous power improvement in InGaN V-Shaped Quantum Well LED using CSG on SiC Substrate	IOP Conference Series: Materials Science and Engineering,	doi:10.1088/1757-899X/906/1/012011
3	Dr. D. Nirmal Associate Professor	AlGaN/GaN HEMT for highly sensitive detection of Bio-molecules using transconductance method	IOP Conference Series: Materials Science and Engineering,	doi:10.1088/1757-899X/872/1/012048
4	Dr. D. Nirmal Associate Professor	Strain-Induced Ionic Polarization Dependent AlGaN/GaN High Electron Mobility Transistor	Proceedings of the 4th International Conference on Trends in Electronics and Informatics, ICOEI 2020, 2020, pp. 463-466, 9142918	SCAD College of Engineering and Technology – 15-17 June 2020, pp. 463-466, 9142918
5	Sam Paul, P., Shylu, D.S	Study on the Influence of Auxiliary Mass on Displacement Using Computational Static Analysis	International Virtual Conference on Emerging Trends in Design, Manufacturing, Materials and Thermal Sciences, ETDMMT 2020	Virtual Online