

Faculty Profile

A. Josephine Anucia

Assistant Professor,

Department of Computer Science and Engineering

email id: josephineanucia@karunya.edu



Academic Background

Degree	University	Year
Ph.D Nano Electronics	Karunya Institute of Technology and Sciences Karunya Deemed University	2022 (Thesis Submitted)
M.Tech VLSI Design	Karunya Institute of Technology and Sciences Karunya Deemed University	2018
B.Tech ECE	Karunya Institute of Technology and Sciences Karunya Deemed University	2016

Research Interests

- Device Modelling
- Low Power VLSI Design
- Digital Electronics
- HDL

Most recent Publications

Conference

1. D. Jackuline Moni, **A. Josephine Anucia**, D. Gracia, D. Nirmal (2017), "TCAD Simulation Study of GaSb/InAs Tunnel FET for Low Power Applications", International Symposium on Nano Materials for Clean Energy and Health Applications (ISNCHA 2017), Coimbatore Institute of Technology, 6-8 December.
2. D. J. Moni, **A. Josephine Anucia**, D. Gracia, and D. Nirmal (2018), "Performance Analysis of GaSb/InAs Tunnel FET for Low Power Applications," Proc. 4th Int. Conf. Devices, Circuits Syst. ICDCS 2018, pp. 335–338, 2019, doi:
[10.1109/ICDCSyst.2018.8605119](https://doi.org/10.1109/ICDCSyst.2018.8605119).

3. **Josephine Anucia, A.**, Jackuline Moni, D., Gracia, D. (2022), “Investigation of Gate-all-around p-type Dual Metal Double Gate Silicon Nanotube FET”, Proc. 6th Int. Conf. Devices, Circuits Syst. ICDCS 2022, Karunya Institute of Technology and Sciences.
4. Angelin Delighta. A., Jackuline Moni, D., Gracia, D., **Josephine Anucia, A.**, (2022), “Dual Material Gate Junctionless Field Effect Transistor for biosensing application”, Proc. 6th Int. Conf. Devices, Circuits Syst. ICDCS 2022, Karunya Institute of Technology and Sciences.

Book Chapter

1. **Josephine Anucia, A.**, Jackuline Moni, D., Gracia, D. (2021), “RF Analysis of Silicon Nanotube FET for Ultra-Low-Power Applications”, Lecture Notes in Electrical Engineering, 700, 2037–2044. https://doi.org/10.1007/978-981-15-8221-9_189 (Book Chapter)

Journals

1. **Josephine Anucia A.**, Jackuline Moni D., Gracia D. (2021), “DC and RF analysis of Vertical 3D p-type Silicon Nanotube FET for low power applications,” International Journal of Electronics, Volume 109, No. 4, pp 721-732; DOI: [10.1080/00207217.2021.1941288](https://doi.org/10.1080/00207217.2021.1941288).
2. **Josephine Anucia A.**, Gracia D., Jackuline Moni D. (2022), “Comparative Analysis of Vertical Nanotube Field Effect Transistor (NTFET) Based on Channel Materials for Low Power Applications”, WSEAS Transactions on Circuits and Systems, Volume 21, pp 26-33; <https://doi.org/10.37394/23201.2022.21.3>.