ALFRED KIRUBARAJ. A
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RESEARCH/TEACHING INTERESTS

Digital System design using VHDL VLSI Design, Network Theory Electric Circuits Electron Devices, Basic Electronics, CAD for Electronics Engineer, Semiconductor memory design and testing, Hardware Verification Techniques, Testing of VLSI circuits, CAD for VLSI circuits, CMOS VLSI Design, Advanced Memory Design, Digital IC Design, Electronic circuits, Network Theory, Internet of Things, Laser Interference Lithography, Flexible Electronics, Fabrication of flexible super-capacitor, Plasmonic Grids, Advanced Memory Design-MRAM, FinFET Technology.

EXPERIENCE

Assistant Professor, Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, Coimbatore, India, 2011 – present

Lecturer, Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, Coimbatore, India, 2009 – 2011

EDUCATION

Degree	Branch / Specialization	University	Class	Mode	Month & Year of Passing
Ph.D.,	Electronics and Communication - Nanotechnology	Karunya Institute of Technology and Sciences	First Class	Part Time	Dec 2019
M.Tech.,	VLSI Design	SRM University	First Class	Full Time	May 2009
B.E.,	Electrical and Electronics Engineering	Anna University	First Class	Full Time	April 2007

SUMMARY OF INTERNATIONAL JOURNAL& CONFERENCE PUBLICATIONS – [PUBLISHED & ACCEPTED]

Year	International Journal Publications	International Conference Publications	National Conference publications
2009 - 2021	**9**	**8**	**3**

RESEARCH PROJECTS

#	Tittle of the project	Funding Agency	Amount (Rs.)	Year
1	Design and Fabrication of Symmetric and Asymmetric Nano Structures Using Laser Interference Lithography	KITS	40000	2012-2013
2	The Axis Draw Pen – An Approach for Precision, Skilled and Unmistakable pen	KITS	25000	2017-2018

RESEARCH GUIDANCE

Research guidance as supervisor	Completed	Ongoing
Doctor of Philosophy - PhD Thesis advising	-	1
Master of Engineering - Master's Thesis advising	8	-

AWARDS/HONORS

1. Best Paper Award in Manipal University on "Compact modeling of SRAM using MTJ".
   Best paper award in PSG Tech on "Design of FinFET in 50nm technology with hybrid mode (IG/LP)".